Design and Optimization of Robust Process Monitors

[1]Shiva Sharma*, [1]Koushik De*, [1]Bhartipudi Sahishnavi, [2]Khanh M Le, and [1,2]Zia Abbas
[1]International Institute of Information Technology, Hyderabad, India, [2]Analog Intelligent Design, Inc., CA, USA
Email(s):(shiva.sharma, koushik.de)@research.iiit.ac.in, kml@aianalog.co, zia.abbas@iiit.ac.in
*These authors have equal contribution

2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS) | 979-8-3503-8717-9/24/$31.00 ©2024 IEEE | DOI: 10.1109/MWSCAS60917.2024.10658748

***Abstract*—This paper presents a new approach to efficient process monitor (PMON) design. It focuses on robust process tracking of PMOS and NMOS devices while minimizing the effects of external factors such as die temperature variations and local supply voltage changes. The proposed design method introduces a comprehensive set of PMON libraries tailored for the specific device types provided by a target technology node. Central to this method is a novel design automation routine based on Zero Temperature Coefficient (ZTC) biasing of a ring oscillator-based PMON. This work demonstrates the effectiveness and scalability of the proposed method across multiple process nodes. The generated PMON structures show a multi-fold improvement in sensitivity for process tracking compared to current state-of-the-art solutions.**

***Index Terms*—Process monitor(PMON), ZTC, Ring oscillator(RO), Temperature Coefficient(TC), Real-time optimization**

I. Introduction

The efficacy of process monitors profoundly impacts integrated circuit (IC) production, influencing production quality, yield, and overall efficiency. Accurately monitoring and adapting system performance to semiconductor manufacturing process variations is crucial for ensuring consistent performance and reliability. However, traditional process monitoring approaches often encounter challenges from external factors such as die temperature variation and local supply voltage changes, which can introduce significant uncertainties and complexities into the monitoring process [1], [2]. As semiconductor technology advances, process monitors (PMON) with reduced sensitivity to these external factors become critical. This research paper delves into the requirements and develops a new methodology to create effective semiconductor process monitors that exhibit minimal coupling to external factors while maximizing their connection to device parameter movement, ultimately aiming to enhance the precision and efficiency of the manufacturing process.

A. Background and related work

In most cases, dummy MOSFETs are strategically placed at various points on the wafer to gain insights into the inconsistencies of the chip manufacturing process, as shown in Fig. 1 [3]. For process monitoring, current is injected into the dummy MOSFET devices. The transconductance(g_m) versus drain current(I_d) graph is observed, and the threshold voltage is calculated from it. However, the application of dummy MOSFETs for process monitoring increases the complexity and manufacturing time potentially adding costs.

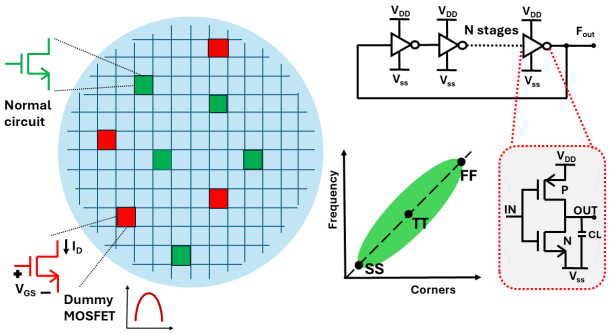


Fig. 1: Process variation across wafer dummy MOSFETs and ring oscillator used for process monitoring

The ring oscillator, as shown in Fig. 1, is well known for its simple structure and is widely used in process monitoring applications due to its effectiveness [4]. Efforts in recent literature have focused on extending the Zero Temperature Coefficient (ZTC) concept to ring oscillators to reduce temperature-induced variability in process sensors [5], [6]. The ZTC theory states that in MOSFET, specific device parameters, such as threshold voltage or mobility, exhibit minimal temperature dependence at a specific operating point [7]–[10].

Previous research [7], [8], [11] has attempted to derive the ZTC operating point for individual MOSFET devices, relying on empirical models or simplistic assumptions about device behavior. Despite the well-established theoretical foundation of ZTC [8]–[10], translating this concept into practical, reliable CMOS process monitoring tools encounters a significant challenge, especially in advanced technology nodes, due to their greater sensitivity to process variations.

These variations significantly impact device characteristics, complicating the accurate identification of the ZTC operating points. In their recent work, cited as [5] and [6], researchers have demonstrated a novel application of ring oscillator-based PMON to detect the ZTC voltages of PMOS and NMOS MOSFETs within various technology nodes. Through comprehensive simulations, these studies aimed to establish the ZTC voltages for each MOSFET type individually and subsequently averaged these values to specify the ZTC operating point of the ring oscillator. However, these works do not demonstrate any proof point optimizing the PMON in terms of its temperature and voltage coupling to the output frequency.

TABLE I: Results of PMON from reference design in 180nm

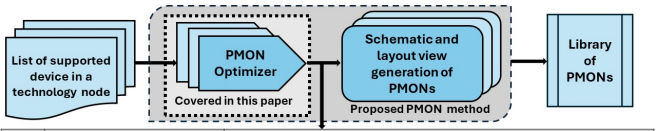
Parameter	Existing Literature	Our work
Number of Stages (N)	5, 9, 15	3
Beta (P/N ratio)	2.7/1	7/2
Nmos (V_{ZTC})	0.847V	0.847V
Pmos (V_{ZTC})	1.17V	1.17V
Average (V_{ZTC})	1V	1V
Temperature Coefficient (TC)	>1400ppm/°C	**15.38ppm/°C**
Voltage Coefficient (VC)	>2.43%/mV	**0.24%/mV**

B. Motivation for better PMON optimizer

Therefore, a robust PMON that overcomes limitations observed in designs from published papers is needed. While these designs may show some performance, they did not confirm the optimal parameter combinations. Existing methodologies for ZTC derivation did not rigorously demonstrate that the selected parameters will result in the most efficient and effective PMON. Without a comprehensive and systematic approach to ZTC calculation, the significant risk of suboptimal performance and inefficiencies in identifying proper process bins remains. Thus, our study focuses on developing a robust design framework that can accurately guide the design and optimization of PMONs. Table I depicts the implementation of a particular design on a 180nm technology node using the current method. It reveals significant limitations. The Temperature Coefficient (TC) exhibits considerable variation, ranging from 1417 to 1468 ppm/°C across multiple combinations of the number of stages and the P/N ratio of the inverter stages in ring oscillator [12]. While this result offers insights into the TC behavior, it fails to conclusively determine whether a configuration with 15 stages and a P/N ratio of 2.7 yields the best TC compared to other potential design parameter combinations. Furthermore, the implementation does not provide the Voltage Coefficient (VC) of the ZTC point of 1V. The above results suggest there is a need for a systematic approach to considering critical design parameters in finalizing the PMON design. Consequently, Section II explains the concept of the proposed methodology for the PMON design, while Section III provides details about the experimental results, and Section IV presents the conclusion and future works.

II. Proposed Method of Process Monitor Design

Fig. 2 illustrates the broad design framework of a PMON library designed for specific device variants supported by a technology platform. Initially, the framework receives input comprising a list of devices, directing them to a PMON optimizer module. The output generated by this optimizer which is the specification table in Fig. 2, includes a comprehensive list of optimized parameters of the PMON, including ZTC bias voltage, the number of stages (N), and the P/N ratio for each stage, other optimized parameters include PMON gain, offset, TC, and VC.



S. No	PMON optimizer output	Justification of the measures for PMON
1	V_{ZTC}	ZTC Bias voltage for PMONs
2	Number of stages (N)	Number of stages with ring oscillator
3	β (Beta)	P/N ratio of INV stage for a specific device type ring oscillator
4	Temp. Coefficient (TC)	Useful in-case needed to calibrate die temperature impact
5	Voltage Coefficient (VC)	Useful in-case needed to calibrate local voltage drop impact
6	Freq. of operation (F_{osc})	Required for converters (like FDC or TDC)
7	Gain and offset	Process monitor gain and offset across overall process window
8	Power consumption	Needed to get power budgeting of a system (active and power down)

Fig. 2: Proposed design framework of PMON library

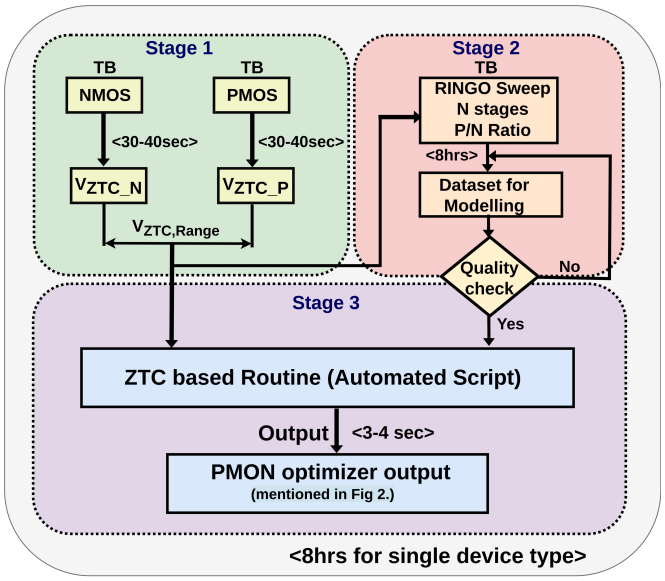


Fig. 3: Design stages of proposed PMON optimizer

By analyzing various design parameter combinations, the optimizer identifies the optimal configuration yielding the best gain while minimizing other specifications such as offset, TC, and VC. These critical performance metrics are useful to system designers for potential PMON calibration in environments with known die temperature and local voltage drop. Additionally, it furnishes information including operating frequency and frequency gain across the process window, which is crucial for calculating process monitoring resolution with a frequency-to-digital converter. Moreover, the optimizer also provides the PMON's power consumption in active and shutdown states imperative for accurate system power budgeting. This systematic analysis and reporting of PMON characteristics represent a novel contribution, as none of the previously referenced papers explored, captured, or reported such details for the PMONs.

The proposed PMON optimizer module and its design flow, as illustrated in Fig. 3, consists of three stages of operation. Stage-1 starts with running test benches to independently determine the ZTC voltage for PMOS and NMOS devices via simulation. This stage typically takes about 30 to 40 seconds

TABLE II: Results of PMON optimiser for 28nm

Device Type	ULVT	LVT	Normal VT	HVT
NMOS (V_{ZTC})	680mV	645mV	760mV	810mV
PMOS (V_{ZTC})	604mV	653mV	800mV	848mV
Inverter (V_{ZTC})	760mV	780mV	860mV	880mV
Temperature Coefficient (TC)	7.97ppm/°C	16.7ppm/°C	12.3ppm/°C	79.3ppm/°C
Voltage Coefficient (VC)	0.32%/mV	0.19%/mV	0.18%/mV	0.23%/mV
No. of Stages (N)	9	17	5	21
Beta (P/N ratio)	5/1	9/1	8/7	2/2
Gain at TT, 27°C	6.59	2.04	3.27	2.05
Leakage Power	413µW	446µW*	20µW	2.3µW
Active Power	58mW	74mW	132mW	46mW

* LVT devices consume more Leakage power than ULVT due to the higher number of stages.

in real computer time. This initial step significantly narrows the range for accurately determining the ZTC point. Upon establishing the initial range of ZTC voltage, the simulation range is further refined to incorporate values exceeding the PMON's ZTC voltage to identify the accurate operating point exhibiting the minimum TC.

A. Generation of the Dataset: Methodology and Parameters

Following the initial determination of the bias voltage range of the ring oscillators, Stage-2 involves the generation of a dataset from simulation across process corners and Monte-Carlo simulations. Prior research has shown that the frequency of ring oscillators is directly proportional to the number of stages (N), the Beta (β, P/N ratio), and the supply voltage (VDD) of the oscillator. [13], [14] With the voltage range already optimized to focus the analysis, the dataset is generated around these critical variables. An extensive parameter sweep is conducted β values varying from 0.1 to 9 and with N from 3 to 23. This compute-intensive stage depends on capabilities of the computer hardware and typically takes about 6-8 hours for a single device type PMON optimization. The resultant dataset covers the temperature range from $-40°\mathrm{C}$ to $125°\mathrm{C}$.

B. Derivation of optimized PMON parameters

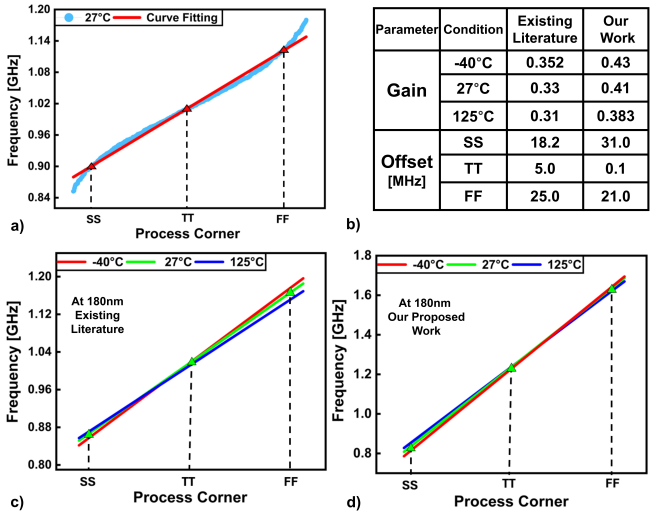
The generated dataset from Stage-2 goes through a detailed quality check (QC) before getting into Stage-3. During QC, several data consistency patterns are checked. Following the QC, an inbuilt script is executed to calculate the minimum TC for each set of combinations from the results of the parameter sweep. This stage takes approximately 3 to 4 seconds to compute. Subsequently, the N and β values corresponding to this minimum TC value are determined. This methodology assesses all the parameters influencing ZTC voltage and is applicable to different types of devices. As illustrated in Table II the TC value for a PMON for the standard VT device is 12.3ppm/°C, achieved for the ring oscillator with 5 stages, and a β of 8/7 for the single inverter stage. The methodology's efficiency is further validated with different device types to confirm the accuracy of the derived ZTC Voltages. In addition, results show the calculated TC values are 7.97ppm/°C and 79.3ppm/°C for Ultra-low VT (ULVT) and High VT (HVT) devices, respectively. These results underscore the robustness and adaptability of the proposed methodology in minimizing temperature sensitivity for the PMONs created from different device types.

III. Experimental Results

Fig. 4 presents a comparison between the results of our proposed PMON optimizer and those from the state-of-the-art design for a ring oscillator-based PMON in 180nm, across the temperature range of $-40°\mathrm{C}$ to $125°\mathrm{C}$. Fig. 4a shows the PMON frequency output across 1,000 global Monte Carlo process corners datapoints at the temperature of $27°\mathrm{C}$. A linear curve fitting method is used to calculate PMON gain and offset parameters. Fig. 4c shows the PMON ring oscillator frequency across process and at temperatures of $-40°\mathrm{C}$, $27°\mathrm{C}$, and $125°\mathrm{C}$ from existing literature. Fig. 4d depicts the results from our proposed methodology. It shows better consistency across temperature and will have minimal impact on the detection of process corners. As shown in Fig. 4b, the PMON from our proposed method also exhibits greater gain and lower offset, desirable for better resolution.

Our results indicate that the gain of the PMON designed using the proposed optimizer surpasses that of the existing literature PMON by a factor of 1.25x, while the offset is reduced by 50x at the typical process corner. Even in the worst-case corner, the gain increases by 1.2x, and the offset is comparable to that of the existing literature. Table I shows that the TC and VC of our proposed optimizer stand at $15.38ppm/°\mathrm{C}$ and $0.24\%/mV$, representing a reduction of over 90x and 10x, respectively to those of a PMON designed with the current method for 180nm technology node.

Table II shows the results of the proposed optimizer, conducted across devices with various VT flavors in 28nm node. From the simulation results, we observe a consistent pattern in ZTC points for most of the devices except for ULVT devices, where the NMOS ZTC value surpasses the PMOS ZTC value. Interestingly, when deriving the ZTC bias point of the inverter unit that forms a stage of a ring-oscillator PMON, we discover that the ZTC value is not around the mid-point of P and N



Parameter	Condition	Existing Literature	Our Work
Gain	-40°C	0.352	0.43
	27°C	0.33	0.41
	125°C	0.31	0.383
Offset [MHz]	SS	18.2	31.0
	TT	5.0	0.1
	FF	25.0	21.0

Fig. 4: PMON optimiser gain and offset at 180nm compared to traditional design

TABLE III: Results from PMON optimiser (Normal VT)

Tech. Nodes	V_{ZTC} [mV]	No. of Stages (N)	Beta (P/N ratio)	TC [ppm/°C]	VC [%/mV]
180nm	1000	3	7/2	15.38	0.24
65nm	870	3	9/7	51.9	0.21
28nm	860	5	8/7	12.3	0.18

Parameter	Condition	For 65nm		For 28nm	
		Existing Literature	Our Proposed Work	Existing Literature	Our Proposed Work
Gain	-40°C	0.745	2.580	1.24	6.72
	27°C	0.685	2.430	1.16	6.38
	125°C	0.627	2.250	1.06	5.8
Offset [MHz]	SS	120	151	1240	350
	TT	70	71	1160	110
	FF	24	17	1060	57

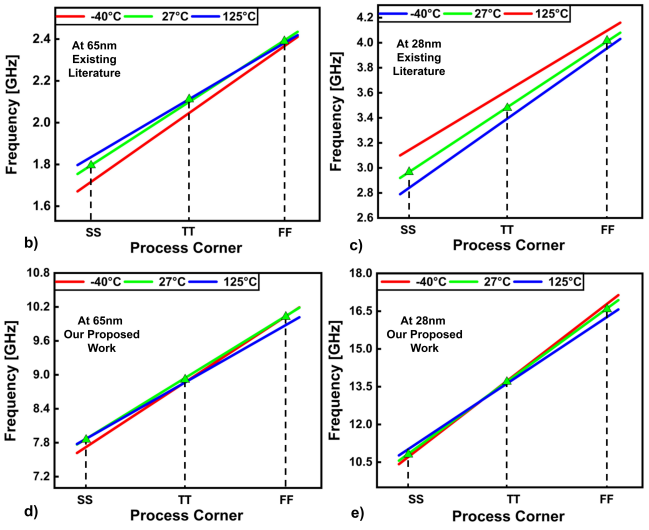


Fig. 5: PMON optimiser results in 65 and 28nm technology nodes compared to traditional design

ZTC values as traditionally assumed in the reference papers. Instead, the proposed routine extends the range until the lowest temperature coefficient value is obtained, deviating from the initial reference point of device-level ZTC.

Additionally, Table II shows that the optimizer yields different β and N values across device types. Results from the optimizer module also shows ULVT devices exhibit the highest PMON gain as expected due to their higher operating frequency. Another significant metric from the optimizer module is the power consumption at the worst corner. Notably, the leakage power in the off-state is higher for LVT PMON due to higher number of stages.

IV. Conclusion and Future Work

The comparison of the proposed optimizer-based PMON performance at lower technology nodes, similar to the analysis conducted at the 180nm node, is further depicted in Fig. 5. It illustrates the Monte Carlo sweep results across 1,000 points, linearized for three extreme temperature cases. Comparisons of gain and offset for PMONs at the 65nm and 28nm nodes with normal VT devices are depicted table in Fig. 5a. With the 65nm node, Fig. 5b and Fig. 5d show a 3.5x increase in gain, and an offset comparable to the traditional PMON design method. Furthermore, a comparison of the frequency output from the traditional PMON ring oscillator in the existing literature with that of our proposed optimizer-driven PMON design is shown in Fig. 5c and Fig. 5e at 28nm technology node. Notably, significant improvements are observed for the 28nm node, like a 5.5x increase in gain and a 10.5x reduction in offset. Overall, Table III provides an overview of the resultant design parameters for PMON with normal VT devices across technology nodes checked within scope of this work and optimized for the lowest TC, and reports its corresponding VC.

This study has introduced an innovative method for ZTC-based process monitor (PMON) design and optimization intended to efficiently track PMOS and NMOS device process variations while providing essential parameters for integration into conventional ASIC designs. The work presented in this paper demonstrates an effective PMON design and optimization framework applicable to multiple process nodes and various flavors of devices that result in improved tracking of process variations compared to the state-of-the-art designs. The gain of the PMON created with this framework is consistently several times higher for all technology nodes without affecting other parameters. The novel framework in this paper produces optimized PMON highly useful for process tracking applications.

Future research will advance the integration of artificial intelligence and machine learning, enabling autonomous adaptation based on real-time feedback. By pursuing these avenues of research, we aim to continuously push the boundaries of process monitor design optimization, enhancing its efficiency, reliability, and performance across various advanced process nodes.

REFERENCES

[1] L. Lisha, O. Bass, and J. Shor, "A 5800 μm² process monitor circuit for measurement of in-die variation of Vth in 65nm," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 863–867, 2021.

[2] D. Mirzoyan and A. Khachatryan, "A new process variation monitoring circuit," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 1–5, 2016.

[3] W. Zhang, X. Li, F. Liu, E. Acar, R. A. Rutenbar, and R. D. Blanton, "Virtual probe: A statistical framework for low-cost silicon characterization of nanoscale integrated circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 12, pp. 1814–1827, 2011.

[4] M. Anees, K. Rahul, S. Swarnkar, and S. Yachareni, "Process monitoring vehicle for sram critical path using ring oscillator in 7 nm FinFet," pp. 1–4, 04 2021.

[5] S. Singhai, A. Kharalkar, and R. Zele, "Process sensor using current-steering logic inverter based ring oscillator," in *2022 IEEE 19th India Council International Conference (INDICON)*, pp. 1–5, 2022.

[6] S.-W. Chen, M.-H. Chang, W.-C. Hsieh, and W. Hwang, "Fully on-chip temperature, process, and voltage sensors," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 897–900, 2010.

[7] S. B. Chiah, X. Zhou, and L. Yuan, "Compact Zero-Temperature Coefficient modeling approach for MOSFETs based on unified regional modeling of surface potential," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2164–2170, 2013.

[8] I. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 7, pp. 876–884, 2001.

[9] L. Najafizadeh and I. Filanovsky, "A simple voltage reference using transistor with ztc point and ptat current source," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, vol. 1, pp. I–909, 2004.

[10] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, "Self-biased CMOS current reference based on the ZTC operation condition," in *2014 27th Symposium on Integrated Circuits and Systems Design (SBCCI)*, pp. 1–7, 2014.

[11] Z. Prijić, S. Dimitrijev, and N. Stojadinović, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectronics Reliability*, vol. 32, no. 6, pp. 769–773, 1992.

[12] P. Toledo, *MOSFET Zero-Temperature-Coefficient (ZTC) Effect Modeling and Analysis for Low Thermal Sensitivity Analog Applications*. PhD thesis, 09 2015.

[13] G. Jovanović, M. Stojcev, and Z. Stamenkovic, "A CMOS voltage controlled ring oscillator with improved frequency stability," *Scientific Publications of the State University of Novi Pazar Series A Applied Mathematics Informatics and mechanics*, vol. 2, pp. 1–9, 06 2010.

[14] M. Mandal and B. C. Sarkar, "Ring oscillators: Characteristics and applications," *Indian Journal of Pure and Applied Physics*, vol. 48, pp. 136–145, 02 2010.